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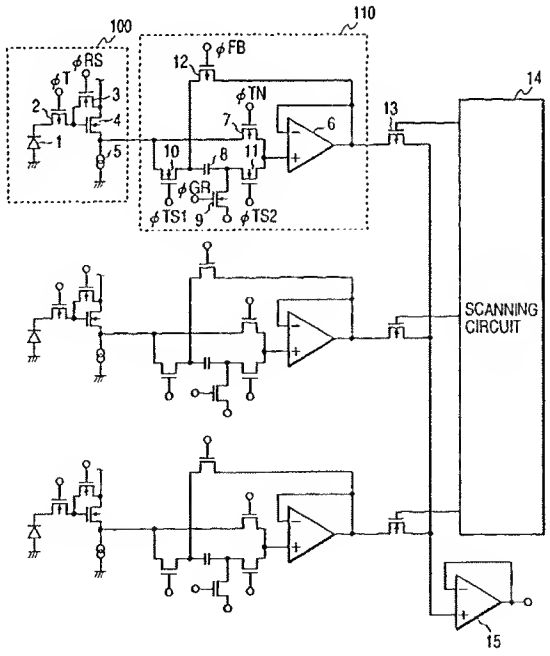
(54) Signal processing apparatus

(57) To realize low noise and chip area reduction, a signal processing apparatus including a signal source, an arithmetic circuit for performing an arithmetic operation, and a non-inverting output circuit for outputting a signal from the arithmetic circuit which includes at least a transfer circuit for transferring a signal from the signal source to the non-inverting output circuit, and a difference signal formation circuit for forming a difference signal obtained by subtracting a signal from the non-inverting output circuit from the signal from the signal source.

FIG. 3



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a signal processing apparatus having a noise removing circuit, a signal processing apparatus for outputting individual signals of a plurality of signal sources and at least the maximum and minimum signals from a plurality of signal sources, and an image pickup apparatus using the signal processing apparatus.

Related Background Art

[0002] Fig. 1 is a signal processing apparatus for sequentially outputting signals.

[0003] Referring to Fig. 1, signals S1, S2,..., Sn are sequentially output to an output line 102 through a non-inverting output circuit (voltage follower circuit) 103 by controlling a MOS transistor 101 by a shift register 100.

[0004] Fig. 2 shows a photoelectric conversion apparatus having a noise removing circuit.

[0005] An amplified photoelectric conversion apparatus is disadvantageous because of large noise generated in pixels and therefore requires a noise removing circuit. Examples of amplified photoelectric conversion apparatus are a BASIS and CMOS sensor. Although Fig. 2 shows a CMOS sensor having a two-dimensional array of photoelectric conversion elements 70, even if the sensor is a linear sensor or a BASIS sensor, a same noise removing circuit is used in those sensors.

[0006] Referring to Fig. 2, the photoelectric conversion apparatus includes horizontal driving lines 71 for controlling lines, vertical output lines 72 for outputting pixel outputs to a noise removing circuit 74, amplified MOS transistors 73 of the pixels 70, load MOS transistors, and a constant current source. The noise removing circuit 74 is generally called an S-N noise removing circuit and comprises capacitances C_{TN} 77 for storing N charges, capacitances C_{TS} 78 for storing S charges, switch MOS transistors 75 and 76 for the capacitances, and horizontal driving MOS transistors 79 and 80 driven by a horizontal scanning circuit 85. An S signal and N signal are input to a differential amplifier 84 through voltage follower circuits 82 and 83, respectively, to remove noise and are output from the noise removing circuit. Let V_P be the optical output from the pixel 70, V_N be noise, C_T be the storage capacitance value, and C_H be the parasitic capacitance of the horizontal output line. Then, a final output V_{OUT} is given by

$$V_{out} = \frac{C_T}{C_T + C_H}\{(V_P + V_N) - V_N\} = \frac{C_T}{C_T + C_H}V_P$$

[0007] However, the prior arts have the following problems.

[0008] In the prior art shown in Fig. 1, since a signal is output through the non-inverting output circuit, the noise signal (e.g., offset signal) from the non-inverting output circuit is added and output together with the signal.

[0009] The prior art shown in Fig. 2 has the following problems:

(1) Since two large MOS capacitances are formed, the chip area increases. Especially, as the device shrinks in feature size, most area is occupied by the MOS capacitances, resulting in a serious problem.
(2) When the S capacitance value shifts from the N capacitance value, the noise correction effect degrades (variation in C_T).
(3) The sensitivity decreases to $C_T/(C_T + C_H)$ because of the capacitance division ratio of the storage capacitance to the parasitic capacitance.

SUMMARY OF THE INVENTION

[0010] It is the first object of the present invention to read out an accurate signal free from noise.

[0011] It is the second object of the present invention to reduce the chip area.

[0012] In order to achieve the above object, according to an aspect of the present invention, there is provided a signal processing apparatus comprising a signal source, a non-inverting output circuit for outputting a signal from the signal source, and noise signal removal means for, when the signal from the signal source is output from the non-inverting output circuit, removing a noise signal in the non-inverting output circuit and causing the non-inverting output circuit to output the signal from the signal source.

[0013] According to another aspect, there is provided a signal processing apparatus comprising a signal source, arithmetic means for performing an arithmetic operation, and a non-inverting output circuit for outputting a signal from the arithmetic means, wherein the arithmetic means including at least transfer means for transferring a signal from the signal source to the non-inverting output circuit, and difference signal formation means for forming a difference signal obtained by subtracting a signal from the non-inverting output circuit from the signal from the signal source.

[0014] According to still another aspect, there is provided a signal processing apparatus comprising a plurality of signal sources, a non-inverting output circuit for outputting signals from the plurality of signal sources, specific value signal output means for causing the non-inverting output circuit to output a maximum or minimum signal of at least two of the plurality of signal sources, and noise signal removal means for, when the signal from the signal source is output from the non-inverting output circuit, removing noise signal in the non-inverting output circuit and causing the non-inverting output cir-

cuit to output the signal from the signal sources.

[0015] According to still another aspect, there is provided a signal processing apparatus comprising a plurality of signal sources, specific value detection means for outputting a maximum or minimum signal of the plurality of signal sources, the specific value detection means having a function of sequentially outputting individual signals from the plurality of signal sources, and driving means for switching the function of the specific value detection means.

[0016] According to still another aspect, there is provided a signal processing apparatus comprising a plurality of signal sources, maximum detection means for outputting a maximum signal of the plurality of signal sources, minimum detection means for outputting a minimum signal of the plurality of signal sources, the maximum or minimum detection means having a function of sequentially outputting individual signals from the plurality of signal sources, and driving means for switching the function of the maximum or minimum detection means having the function of sequentially outputting the individual signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

Fig. 1 is a circuit diagram showing the first prior art;
Fig. 2 is a circuit diagram showing the second prior art;
Fig. 3 is a circuit diagram showing the first embodiment of the present invention;
Fig. 4 is a timing chart of the first embodiment of the present invention;
Fig. 5 is a circuit diagram showing the second embodiment of the present invention;
Fig. 6 is a circuit diagram showing the third embodiment of the present invention;
Fig. 7 is a circuit diagram showing the fourth embodiment of the present invention;
Fig. 8 is a circuit diagram showing the fifth and sixth embodiments of the present invention;
Figs. 9A and 9B are circuit diagrams showing examples of a differential amplifier used in the present invention;
Fig. 10 is a circuit diagram showing the seventh embodiment of the present invention;
Fig. 11 is a circuit diagram showing the eighth embodiment of the present invention;
Fig. 12 is a circuit diagram showing the eighth embodiment of the present invention;
Fig. 13 is a timing chart of the eighth embodiment of the present invention;
Fig. 14 is a timing chart of the eighth embodiment of the present invention;
Fig. 15 is a circuit diagram showing the ninth embodiment of the present invention;
Fig. 16 is a circuit diagram showing the 10th embodiment of the present invention;
Fig. 17 is a circuit diagram showing the 11th embodiment of the present invention;
Fig. 18 is a circuit diagram showing the 12th embodiment of the present invention;
Fig. 19 is a circuit diagram showing the 13th embodiment of the present invention; and
Fig. 20 is a circuit diagram showing the 20th embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] Fig. 3 shows the first embodiment which most clearly presents the characteristic feature of the present invention. Referring to Fig. 3, a pn photodiode 1 performs photoelectric conversion. A transfer gate 2 transfers photoelectrically converted charges. A reset MOS transistor 3 resets charges. An amplified MOS transistor 4 and constant current source 5 form a source follower circuit. The above components 1 to 5 construct one photoelectric conversion pixel. A differential amplifier 6 feeds back its output to the negative input terminal to perform voltage follower operation. A switch MOS transistor 7 inputs the output from the photoelectric conversion pixel to the voltage follower circuit. A clamp capacitance 8 and switch MOS transistor 9 for inputting the clamp potential construct a clamp circuit. A switch MOS transistor 10 inputs the output from the photoelectric conversion pixel to the clamp circuit. A switch MOS transistor 11 connects the clamp circuit and voltage follower circuit. A switch MOS transistor 12 inputs the output from the voltage follower circuit to the clamp circuit. The components 6 to 12 construct a noise removing circuit. A switch MOS transistor 13 outputs the photoelectric conversion output after noise removal to an output amplifier 15 and is driven by a scanning circuit 14.

[0019] The noise removal operation of the present invention will be described next with reference to the timing chart shown in Fig. 4.

[0020] At time t_0, signals ϕRS and ϕT are turned on to reset the photodiode. At time t_1, the signal ϕT is turned off to end reset of the photodiode to start accumulation.

[0021] At time t_2 when noise removal operation starts, signals ϕTN and ϕFB are turned on to input the output from the photoelectric conversion pixel to the voltage follower circuit 6 through the switch MOS transistor 7. The output from the voltage follower circuit is input to the clamp capacitance 8 through the switch MOS transistor 12. At times t_3 and t_4, the switch MOS transistors 12 and 7 are turned off in the order named. At this time, the clamp capacitance 8 holds a voltage as the sum of the sensor output with noise and offset voltage of the voltage follower circuit

$$V_{CP} = V_{dark} + V_{FPN} + V_{RN} + V_{off} \quad (1)$$

(V_{dark} = sensor dark voltage, V_{FPN} = fixed pattern noise voltage, V_{RN} = random noise voltage, and V_{off} = offset voltage of voltage follower circuit)

At time t_5, a signal $\phi TS2$ is turned on to connect the clamp circuit to the voltage follower circuit. At time t_6, a signal ϕGR is turned off to end the clamp operation.

[0022] At time t_7, accumulation starts. After the elapse of a predetermined time, the signal read operation starts at times t_8 and t_9. At time t_8, the signal ϕRS is turned off, and then, at time t_9, the signal ϕT is turned on to transfer charges generated in the photodiode to the gate of the amplified MOS transistor 4 of the source follower circuit. The change in potential at this time is output as an optical signal.

[0023] The output from the source follower is represented by

$$V_P + V_{dark} + V_{FPN} + V_{RN} \quad (2)$$

where V_P is the optical signal voltage. This voltage is input to the clamp circuit through the switch MOS transistor 10. Because of the difference between this voltage and the already stored voltage (1), the output from the voltage follower circuit is given by

$$V_{OUT} = (2) - (1) + V_{off} = V_P$$

That is, a signal from which not only noise of the photoelectric conversion pixel but also noise of the voltage follower circuit are removed can be obtained from the voltage follower circuit. In addition, since the signal can be output to the output amplifier 15 at the final stage without decreasing the gain, the gain does not decrease due to capacitance division.

[0024] Conventionally two large capacitances are required to prevent the decrease in gain due to capacitance division. However, in the present invention, a capacitance 1/2 or less that of the prior art suffices, so the capacitance area can be reduced to 1/4 or less that of the prior art. The clamp capacitance value necessary in the present invention is preferably set in consideration of the ratio of the input capacitance to parasitic capacitance of the voltage follower.

[0025] As described above, according to the first embodiment, a high-sensitivity sensor with a small chip area corresponding to micropatterning can be realized. Particularly, this sensor has a tremendous effect as an AF sensor for a camera which requires real-time AGC because a nondestructive read is possible.

[0026] Fig. 5 shows the second embodiment of the present invention. In this embodiment, the present invention is applied to an AMI (Amplified Mos Imager) sensor which directly inputs the output from a photodiode to the gate of the amplified MOS transistor of a source follower circuit. In this embodiment, the same noise removing circuit as in the first embodiment is arranged, and the same effect as in the first embodiment can be obtained. In this embodiment, NMOS transistors are used in a photoelectric conversion pixel. However, the same effect as described can be obtained even in use of PMOS transistors, as in the first embodiment.

[0027] Fig. 6 shows the third embodiment of the present invention. In the sensor of this embodiment, a pixel has a source follower circuit with a two-stage structure, and the gate of the second source follower circuit has a memory capacitance. When this sensor is used as a contact sensor, the chip area can be made much smaller than that of the prior art. Hence, the cost can be largely reduced. Especially, this sensor is effective as a contact sensor of an equal magnification type.

[0028] In the present invention, transistors in a photoelectric conversion pixel can be formed from either NMOS transistors or PMOS transistors. Alternatively, NMOS transistor are used for the first stage while PMOS transistors are used for the second stage, or vice versa.

[0029] Fig. 7 shows the fourth embodiment of the present invention. The present invention uses a pixel in which the output from a photodiode is input to a voltage follower circuit with a CMOS structure.

[0030] In the fourth embodiment, since a voltage follower circuit formed from a differential amplifier is used, the FPN of the output from the pixel is small. By combining a noise removing circuit on the output side, noise can be further reduced.

[0031] This embodiment can be applied to a sensor which especially requires small noise. Particularly, the sensor is effective as an AF sensor for a camera.

[0032] In the first to fourth embodiments, the photoelectric conversion pixel is not limited to the above-described type. A photoelectric conversion pixel of a BASIS, CMD, SIT, or FGA may be used. The signal from the photodiode may be output without being amplified.

[0033] Fig. 8 shows the fifth embodiment of the present invention. In this embodiment, the present invention is applied to a two-dimensional photoelectric conversion apparatus. Referring to Fig. 8, photoelectric conversion elements 70 are two-dimensionally arrayed. This embodiment exemplifies a CMOS sensor. However, this embodiment can be applied to the photoelectric conversion pixel of a BASIS, CMD, SIT, or FGA. The signal from the photodiode may be output without being amplified. In this embodiment, since the present invention is applied to a two-dimensional photoelectric conversion apparatus, the same effect as in the linear photoelectric conversion apparatus, e.g., reduction of the chip area and increase in sensitivity can be obtained.

[0034] Figs. 9A and 9B are circuit diagrams showing examples of the differential input circuit 6 used in the present invention. Figs. 9A and 9B show CMOS differential amplifiers. However, a BiCMOS structure may be used. As for the circuit arrangement, the output may be of push-pull type. In other words, any types of differential amplifiers can be used.

[0035] As described above, in the fifth embodiment, noise removing circuits are arranged one for each column. However, noise removing circuits may be arranged one for each photoelectric conversion pixel.

[0036] Fig. 8 also shows the sixth embodiment of the present invention. In this embodiment, the peak signal (maximum or minimum signal) of photoelectric conversion pixels in one row is detected.

[0037] In the fifth embodiment, pulses are sequentially input from a horizontal scanning circuit 14 to switch MOS transistors 13, thereby outputting the signals from the photoelectric conversion pixels. In the sixth embodiment, instead of sequentially inputting pulses from the horizontal scanning circuit to the switch MOS transistors, pulses are simultaneously input to the switch MOS transistors. Signals from the photoelectric conversion pixels of one row are simultaneously output from a voltage follower circuit 6, thereby obtaining the peak signal of the photoelectric conversion pixels in one row. When, a voltage follower circuit using N-type transistors at the output stage, as shown in Fig. 9A, is used, the maximum signal of the photoelectric conversion pixels in one row is obtained. When a voltage follower circuit using P-type transistors at the output stage, as shown in Fig. 9B, is used, the minimum signal of the photoelectric conversion pixels in one row is obtained.

[0038] Assume that the voltage follower circuit shown in Fig. 9A is used for odd columns, and the voltage follower circuit shown in Fig. 9B is used for even columns. In this case, by simultaneously inputting a pulse from the horizontal scanning circuit to the switch MOS transistors 13 of odd columns and then simultaneously inputting a pulse from the horizontal scanning circuit to the switch MOS transistors 13 of even columns, almost the maximum or minimum signal of the photoelectric conversion pixel in one row can be obtained.

[0039] Fig. 10 shows the seventh embodiment of the present invention. In this embodiment, the peak signal (maximum or minimum signal) of photoelectric conversion pixels in one row is detected more accurately than in the sixth embodiment.

[0040] In the sixth embodiment, the maximum signal of odd photoelectric conversion pixels in one row and the minimum signal of even photoelectric conversion pixels in one row are obtained. Hence, an error may occur in a low-resolution sensor.

[0041] In the seventh embodiment, one column parallelly has a voltage follower circuit for detection of maximum (Fig. 9A) and that for detection of minimum (Fig. 9B). When a pulse is simultaneously input from the horizontal scanning circuit to switch MOS transistors connected to the voltage follower circuit for detection of maximum, the maximum signal of photoelectric conversion pixels in one row is output to the horizontal output line. When a pulse is simultaneously input from the horizontal scanning circuit to switch MOS transistors connected to the voltage follower circuit for detection of minimum, the minimum signal of photoelectric conversion pixels in one row is output to the horizontal output line.

[0042] When the horizontal scanning circuit has an arrangement capable of simultaneously inputting a pulse to a plurality of switch MOS transistors or an arrangement capable of sequentially inputting a pulse to a plurality of switch MOS transistors, as in the sixth or seventh embodiment, individual signals from the photoelectric conversion pixels and the maximum and minimum signals of photoelectric conversion pixels in one row can be obtained.

[0043] In the sixth and seventh embodiments, the peak signal of photoelectric conversion pixels in one row is obtained. However, the peak signal of photoelectric conversion pixels in one column may be obtained by simultaneously outputting a pulse from a vertical scanning circuit to all rows. Alternatively, when a plurality of arbitrary pulses are simultaneously output from the vertical and horizontal scanning circuits, the peak signal of an arbitrary area in the photoelectric conversion apparatus can be obtained.

[0044] Fig. 11 is a circuit diagram showing the eighth embodiment. Referring to Fig. 11, a pn photodiode 1 for performing photoelectric conversion, a reset MOS transistor 22 for resetting the potential of the photodiode to V_{RES}, and a differential amplifier 23 construct one photoelectric conversion pixel 103. A clamp capacitance 8 and clamp MOS transistor 9 for inputting a clamp potential form a clamp circuit. The photoelectric conversion apparatus has switch MOS transistors 7, 10 and 11. Each of a differential amplifier 21 for detection of maximum and a differential amplifier 20 for detection of minimum constructs a voltage follower circuit. The apparatus also has a maximum output switch MOS transistor 22, minimum output switch MOS transistor 13, OR circuit 24, scanning circuit 14, and constant current MOS transistors 26 and 27. Fig. 12 shows specific circuit arrangements of the differential amplifiers 21 and 20. As the circuit for detection of maximum, a source follower circuit having NMOS transistors at the final stage is used. As the circuit for detection of minimum, a source follower circuit having PMOS transistors at the final stage is used.

[0045] Signals from the pixels are output to common output lines 30 and 30'.

[0046] The operation of this embodiment will be described next with reference to the timing charts shown in Figs. 13 and 14. The operative state is divided into a reset period (noise removal period), accumulation period (AGC period), and video signal output period. The reset period will be described first. At time T_0, a signal ϕRES is set at high level to reset the potential of the pn photodiode 1. At time T_1, reset of the photodiode is ended. At time T_2 when noise removal starts, signals ϕTN1 and ϕTN2 are set at high level to turn on the switch MOS transistors 7 and 12. The output from the differential amplifier 23 for photoelectric conversion is input to the capacitance 8 of the clamp circuit through the switch MOS transistor 7, maximum detection circuit 21, and switch

MOS transistor 12.

[0047] At times T_3 and T_4, the signals ϕTN1 and ϕTN2 are set at low level to turn off the switch MOS transistors 12 and 7. At times T_5 and T_6, a signal ϕTS2 is set at high level to turn on the switch MOS transistor 11, and a signal ϕGR is set at high level to turn off the clamp MOS transistor 9.

[0048] The clamp capacitance 8 holds a voltage as the sum of the noise component in the pixel and the offset component of the differential amplifiers 21 and 20. With the above process, the reset period for removing noise (offset) of the photoelectric conversion section, maximum detection section, and minimum detection section by clamping is ended.

[0049] At time T_7 when the accumulation period (AGC period) starts, signals ϕPEAK and ϕBTM are set at high level to turn on the switch MOS transistors 22 and 13. The outputs from the differential amplifiers 21 and 20 connected to pixels which will output the maximum and minimum are connected to the common output lines 30 and 30' to activate the constant currents 26 and 27.

[0050] When the signals ϕPEAK and ϕBTM are turned on to commonly connect the differential amplifiers 21 and 20 constructing the voltage follower circuits to the output lines 30 and 30', respectively, the output voltage of a pixel for outputting the maximum in the plurality of pixels is output to the common output line 30, and the output voltage from a pixel for outputting the minimum is output to the common output line 30'.

[0051] The voltage held by the clamp capacitance 9 is given by

$$V_{CP} = V_{dark} + V_{RN} + V_{off} \quad (1)$$

(V_{dark} = pixel dark voltage, V_{FPN} = fixed pattern noise voltage, V_{RN} = random noise voltage, and V_{off} = offset voltage of voltage follower circuit)

[0052] The output of the maximum or minimum from the pixel is represented by

$$V_{PB} + V_{dark} + V_{FPN} + V_{RN} \quad (2)$$

where V_{PB} is the maximum or minimum voltage. This voltage is input to the clamp circuit through the switch MOS transistor 11. Because of the difference between this voltage and the already stored voltage (1), the output from the differential amplifiers 21 and 20 is given by

$$V_{OUT} = (2) - (1) + V_{off} = V_{PB}$$

That is, a signal from which not only noise of the photoelectric conversion pixel but also noise (offset component) of the differential amplifiers can be obtained from the amplifier.

[0053] At this time, constant current MOS transistors 28 and 29 on the output sides of the differential amplifiers 21 and 20 are turned off by setting a potential VC2 at low level and potential VREF2 at high level. When the accumulation time has elapsed, and (maximum) - (minimum) reaches a certain value, the AGC operation is ended to end accumulation operation.

[0054] From time T_9, the video signal read period starts. At time T_9, the potential V_{REF2} is set at a set potential (potential at which a desired current is obtained) to activate and operate the constant current MOS transistor 28 of the differential amplifier 20. At time T_{10}, the scanning circuit 14 is scanned to sequentially output signals ϕH1, ϕH2, and ϕH3, thereby serially outputting a video signal.

[0055] With the above operation timing, the minimum detection circuit can have a video signal output function.

[0056] In this embodiment, a voltage follower circuit whose final stage is formed from a source follower is used in units of pixels. In outputting the minimum, the constant current source on the output side of each voltage follower is turned off to commonly connect the voltage follower circuits to the output lines connected to the constant current source, thereby obtaining the minimum of the video signal. In outputting a video signal, the constant current source on the output side of each voltage follower is turned on to sequentially connect the voltage follower circuits to the output lines, thereby obtaining a serial video signal

[0057] In this embodiment, by decreasing the number of circuits, the chip area can be reduced as compared to the prior art. In addition, since the offset removal operation is performed, or the minimum output circuit and video signal output circuit are formed from the same circuit, the output offset can also be reduced.

[0058] In this embodiment, the final stages of the voltage followers of the differential amplifiers 21 and 20 are formed from source follower circuits that use MOS transistors. However, even when an emitter follower circuit using bipolar transistors is used, as in the prior art, the same effect as described above can be obtained.

[0059] Fig. 15 is a circuit diagram showing the ninth embodiment of the present invention.

[0060] In the eighth embodiment, the minimum detection circuit has the video signal output function. In the ninth embodiment, a maximum detection circuit has a video signal output function.

[0061] In this embodiment as well, the chip area can be reduced, and the output offset can be decreased, as in the eighth embodiment.

[0062] Fig. 16 is a circuit diagram showing the 10th embodiment of the present invention.

[0063] In this embodiment, the noise clamp circuit on the input side of maximum and minimum detection circuits is omitted. Accordingly, the output offset as noise increases. However, since the chip area can be largely reduced, this embodiment is effective for a photoelectric conversion apparatus which puts priority on cost rather

than performance.

[0064] Fig. 17 is a circuit diagram showing the 11th embodiment of the present invention.

[0065] In this embodiment, in an inexpensive system using a photoelectric conversion apparatus for outputting only the maximum and video signal, signals may be processed without using the minimum. In this case, by imparting the video signal output function to the maximum detection circuit, as in this embodiment, the number of circuits can be further decreased, and the chip area can be further reduced. In addition, the clamp circuit may be omitted, as in the tenth embodiment.

[0066] According to this embodiment, a more inexpensive photoelectric conversion apparatus can be realized.

[0067] Fig. 18 is a circuit diagram showing the twelth embodiment of the present invention. In this embodiment, photoelectric conversion pixels are two-dimensionally arrayed, and maximum and minimum detection circuits are arranged one each for each column.

[0068] A photoelectric conversion pixel 105 comprises a pn photodiode 1 for performing photoelectric conversion, a transfer MOS transistor 30 for transferring signal charges of the pn photodiode, an amplified MOS transistor 32 for amplifying the transferred signal and outputting it, a reset MOS transistor 31 for resetting the transferred signal to a predetermined reset potential, and a selection MOS transistor 33 for selecting the pixel. A constant current source 37 forms a source follower with an amplified MOS transistor. The photoelectric conversion apparatus also has a vertical output line 35, a vertical scanning circuit 36 for sequentially selecting pixels ot one row, a horizontal output line 38, and a horizontal scanning circuit 39 for sequentially transferring a signal. The same reference numerals as in Fig. 11 denote the same parts in Fig. 18.

[0069] In this embodiment, pixels are selected by the vertical scanning circuit 36 in units of rows, and the same operation as in the first embodiment is performed, thereby obtaining the maximum and minimum outputs and video output of one row.

[0070] The photoelectric conversion pixels in the first to twelfth embodiments are not limited to those described above. For example, the photoelectric conversion pixel described in the twelth embodiment may be used tor the eighth embodiment. In this case, since the eighth embodiment is associated with a line sensor, the selection MOS transistor 33 can be omitted. Any circuit arrangement other than the MOS structure may be used. Not only the MOS structure but also a pixel structure such as a BASIS or SIT may be used. Furthermore, not only a photoelectric conversion pixel for converting light into an electrical signal but also a signal source for generating a voltage signal or the like can be used.

[0071] In the first to 12th embodiments, the output from the clamp circuit 8 or 9 is output through the voltage follower circuit 6, 20, or 21. However, a circuit for doubling the output from the clamp circuit 8 or 9 and outputting it may be used. In this case, the voltage output from the circuit for doubling the signal, which corresponds to the sum of the noise signal voltage from the photoelectric conversion pixel and the offset voltage of the output circuit, is halved by a resistance or the like and input to the clamp circuit 8 or 9.

[0072] Fig. 19 shows the thirteenth embodiment of the present invention. This embodiment presents an image pickup apparatus using the above-described signal processing apparatus shown in the sixth to twelfth embodiments.

[0073] The maximum and minimum signals of photoelectric conversion pixel in one row are output from a photoelectric conversion apparatus 90 shown in Fig. 19, differentially amplified by a differential amplification circuit 91, and input to a comparator 92. The output from the comparator 92 is input to an on-chip or external accumulation time control circuit 93. When the output from the differential amplifier is larger than a reference voltage Vref, the accumulation time control circuit controls the photoelectric conversion apparatus to stop accumulating light. In accordance with stop of light accumulation, signals from the photoelectric conversion pixels are individually output and processed by a signal processing circuit 94 by white balance processing, thereby obtaining an image.

[0074] In this embodiment, pixels are selected by a vertical scanning circuit 36 in units of rows, and the same operation as in the first embodiment is performed, thereby obtaining the maximum and minimum outputs and video output of one row.

[0075] The photoelectric conversion pixels in the eighth to twelfth embodiments are not limited to those described above. For example, the photoelectric conversion pixel described in the 12th embodiment may be used for the eighth embodiment. In this case, since the eighth embodiment is associated with a line sensor, the selection MOS transistor 33 can be omitted. Any circuit arrangement other than the MOS structure may be used. Not only the MOS structure but also a pixel structure such as a BASIS or SIT may be used.

Furthermore, not only a photoelectric conversion pixel for converting light into an electrical signal but also a signal source for generating a voltage signal or the like can be used.

[0076] Fig. 20 is a block diagram showing a specific image pickup apparatus using the signal processing apparatus described in the first to 12th embodiments.

[0077] Referring to Fig. 20, the image pickup apparatus comprises a signal processing apparatus 201 described in the first to 12th embodiments, a differential amplitier 202 for obtaining the difference between a PEAK output V_{PEAK} and BTM output V_{BTM}, a comparator 203 for comparing the output from the differential amplifier 202 with a predetermined reference level V_{ref} and determining that the level has reached an appropriate accumulation level, storage circuits 209 and 211 for storing maximum and minimum signals output from the Vid-

eo line, a differential amplifier 210 for obtaining the difference between the output from the storage circuit 209 and the output from the video output Video, a differential amplifier 212 for obtaining the difference between the outputs from the storage circuits 211 and 209, and a microcomputer 204. The microcomputer comprises a CPU core 204a, ROM 204b, RAM 204c, and A/C converter 204d.

[0078] In the image pickup apparatus shown in Fig. 20, first, the microcomputer 204 outputs reset signals ϕ_{res} and ϕ_{vrs} to start accumulation. Next, in accordance with an inverted signal ϕ_{com} from the comparator 203, the microcomputer 204 outputs a signal ϕ_t to stop accumulation. Also, signals ϕ_{hrs} and ϕ_{ck} are output to read signal charges. At this time, the microcomputer 204 sends a sampling signal SH to the storage circuit 209 at the minimum output timing to store the minimum. The subsequent output from the photoelectric conversion element array is A/D-converted after the difference between the output and the minimum is obtained by the differential amplifier 210. Since a reference potential V_{rl} for A/D conversion is set to be the ground potential and a potential V_{rh} is set to be reference voltage Vref, A/D conversion is performed almost between the maximum and minimum of the output from the photoelectric conversion pixel. However, A/D conversion is accurately performed for a high-contrast portion of an object because the minimum as the reference of the output from the photoelectric conversion apparatus is accurately read out.

[0079] As has been described above, according to this embodiment, the following effects can be obtained.

[0080] A highly accurately signal free from noise can be obtained from a voltage follower circuit.

[0081] Cost can be reduced by reducing the chip area.

[0082] Since the sensitivity is not decreased by capacitance division, a photoelectric conversion apparatus with high S/N ratio can be realized. When this apparatus is used as an image pickup apparatus, photographing at lower luminance than the prior art is possible.

[0083] The simple circuit arrangement can cope with shrinkage in feature size.

[0084] Since multiple reads (nondestructive reads) are possible, the apparatus can be used for various application purposes.

[0085] Since a peak signal is obtained from a plurality of arbitrary signal sources, the apparatus can be used for various application purposes.

[0086] When a peak signal from a plurality of arbitrary photoelectric conversion pixels is used, a clear image can be obtained independently of the contrast of an object.

[0087] Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

Claims

1. A signal processing apparatus comprising:

   a signal source;
   a non-inverting output circuit for outputting a signal from said signal source; and
   noise signal removal means for, when the signal from said signal source is output from said non-inverting output circuit, removing a noise signal in said non-inverting output circuit and causing said non-inverting output circuit to output the signal from said signal source.

2. An apparatus according to claim 1, wherein

   said noise signal removal means also removes a noise signal in said signal source.

3. An apparatus according to claim 2, wherein

   said noise signal removal means adjusts the noise signals in said signal source and said non-inverting output circuit to remove the noise signal in said signal source at an input portion of said non-inverting output circuit and the noise signal in said non-inverting output circuit at an output portion of said non-inverting output circuit.

4. A signal processing apparatus comprising:

   a signal source;
   arithmetic means for performing an arithmetic operation; and
   a non-inverting output circuit for outputting a signal from said arithmetic means,
   said arithmetic means comprising at least transfer means for transferring a signal from said signal source to said non-inverting output circuit, and difference signal formation means for forming a difference signal obtained by subtracting a signal from said non-inverting output circuit from the signal from said signal source.

5. An apparatus according to claim 4, wherein

   said difference signal formation means comprises a clamp circuit.

6. An apparatus according to claim 4, wherein

   said transfer means transfers a noise signal in said signal source.

7. An apparatus according to claim 4, wherein

said difference signal formation means clamps an output signal level output from said non-inverting output circuit to a predetermined potential.

8. An apparatus according to claim 7, wherein

said arithmetic means comprises input means for inputting a signal from said signal source to said clamp circuit after said difference signal formation means clamps the output signal level from said non-inverting output circuit to the predetermined potential.

9. An apparatus according to claim 1 or claim 4, wherein

said signal source comprises photoelectric conversion pixels.

10. An apparatus according to claim 9, wherein

said non-inverting output circuit and said noise signal removal means are provided at an output portion of each photoelectric conversion pixel.

11. An apparatus according to claim 9, wherein

said photoelectric conversion pixels are arrayed in a plurality of rows, and at least one non-inverting output circuit and at least one noise signal removal means are arranged for each vertical output line for outputting an output signal from said photoelectric conversion pixels to a horizontal output line.

12. An apparatus according to claim 11, wherein

the signals from said photoelectric conversion pixels are output to said horizontal output line through said non-inverting output circuit.

13. A signal processing apparatus comprising:

a plurality of signal sources;
a non-inverting output circuit for outputting signals from said plurality of signal sources;
specific value signal output means for causing said non-inverting output circuit to output a maximum or minimum signal of at least two of said plurality of signal sources; and
noise signal removal means for, when the signal from said signal source is output from said non-inverting output circuit, removing a noise signal in said non-inverting output circuit and causing said non-inverting output circuit to output the signal from said signal sources.

14. An apparatus according to claim 13, further comprising

individual signal output means for outputting individual signals from said plurality of signal sources.

15. An apparatus according to claim 13, wherein

said signal sources comprise photoelectric conversion pixels.

16. An apparatus according to any one of claims 1, 4 and 13, wherein

said non-inverting output circuit comprises a voltage follower circuit.

17. An image pickup apparatus comprising:

said signal processing apparatus of claim 15; and
light accumulation amount control means for controlling a light accumulation amount of said photoelectric conversion pixel in said signal processing apparatus in accordance with a peak signal output from said signal processing apparatus.

18. A signal processing apparatus comprising:

a plurality of signal sources;
specific value detection means for outputting a maximum or minimum signal of said plurality of signal sources, said specific value detection means having a function of sequentially outputting individual signals from said plurality of signal sources; and
driving means for switching the function of said specific value detection means.

19. An apparatus according to claim 18, wherein

said driving means switches the function of said specific value detection means by changing a drive timing for causing said specific value detection means to output the signal.

20. An apparatus according to claim 19, wherein

said specific value detection means comprises a plurality of voltage follower circuits connected to said plurality of signal sources, respectively, and
said driving means switches the function by commonly connecting output portions of said

plurality of voltage follower circuits to an output line to output the maximum or minimum signal to said output line and sequentially connecting the output portions of said plurality of voltage follower circuits to said output line to sequentially output the individual signals to said output line.

21. An apparatus according to claim 20, further comprising

a plurality of switch means for connecting the output portions of said plurality of voltage follower circuits to said output line, respectively, said switch means being controlled by said driving means.

22. An apparatus according to claim 20, wherein

said driving means comprises pulse supply means for simultaneously supplying a pulse to said switch means and a scanning circuit for sequentially supplying a pulse to said switch means.

23. An apparatus according to claim 20, wherein the output portion of said voltage follower circuit comprises a source follower circuit.

24. An apparatus according to claim 23, wherein

said output line has a constant current source, and
wherein when the maximum or minimum signal is to be output, a constant current source of said source follower circuit is turned off and said constant current source of said output line is turned on, and
when the individual signals are to be output, said constant current source of said source follower circuit is turned on and said constant current source of said output line is turned off.

25. An apparatus according to claim 19, further comprising

noise removal means for removing noise in said signal sources on an input side of said specific value detection means.

26. An apparatus according to claim 25, wherein

said noise removal means comprises a clamp circuit.

27. An apparatus according to claim 20, wherein

said apparatus further comprises noise removal means on an input side of said voltage follower circuit, said noise removal means removing a noise component level of said signal sources and an offset level in said voltage follower circuit.

28. An apparatus according to claim 19, wherein

said signal sources comprise photoelectric conversion pixels.

29. A signal processing apparatus comprising:

a plurality of signal sources;
maximum detection means for outputting a maximum signal of said plurality of signal sources;
minimum detection means for outputting a minimum signal of said plurality of signal sources,
said maximum or minimum detection means having a function of sequentially outputting individual signals from said plurality of signal sources; and
driving means for switching the function of said maximum or minimum detection means having the function of sequentially outputting the individual signals.

30. An apparatus according to claim 29, wherein

said signal sources comprise photoelectric conversion pixels.

31. An image pickup apparatus comprising:

said signal processing apparatus of claim 30;
comparison means for detecting that a difference value between the maximum signal and the minimum signal output from said signal processing apparatus has not less than a predetermined value; and
control means for controlling a light accumulation time of a photoelectric conversion pixel in said signal processing apparatus on the basis of an output from said comparison means.

FIG. 1

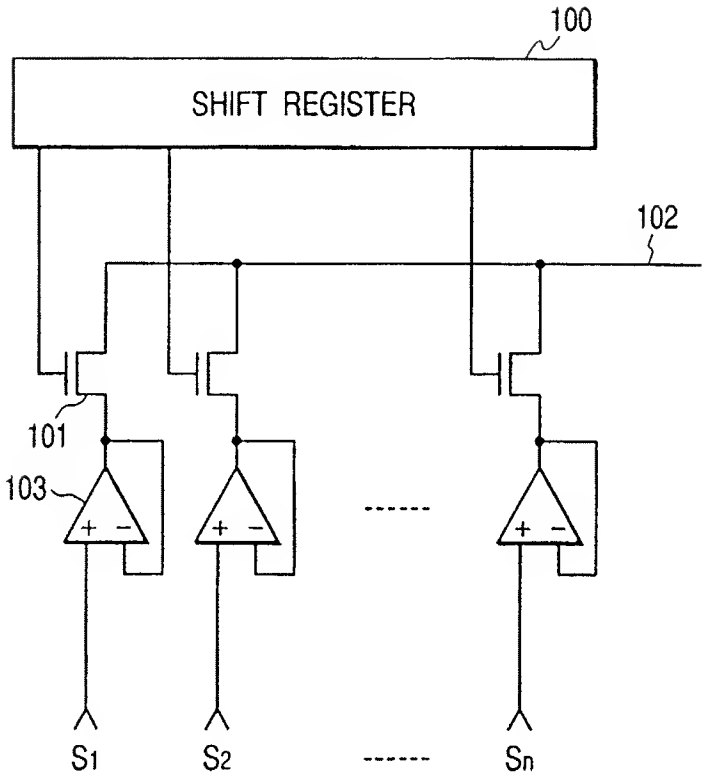


FIG. 2

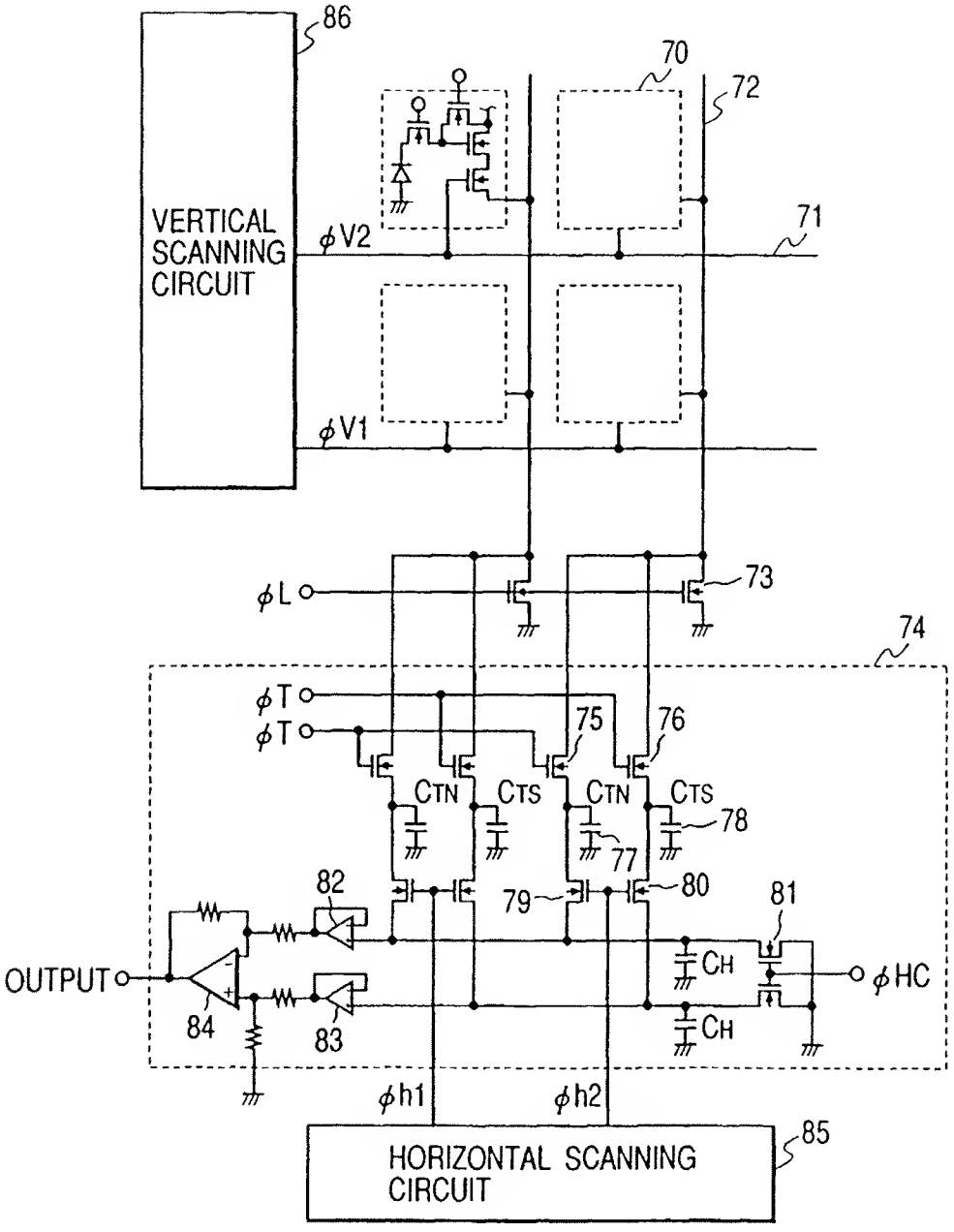

86
70
72
VERTICAL SCANNING CIRCUIT
φV2
71
φV1
φL
73
74
φT
φT
75
76
CTN
CTS
CTN
CTS
78
77
82
79
80
81
OUTPUT
CH
φHC
84
83
CH
φh1
φh2
85
HORIZONTAL SCANNING CIRCUIT

FIG. 3

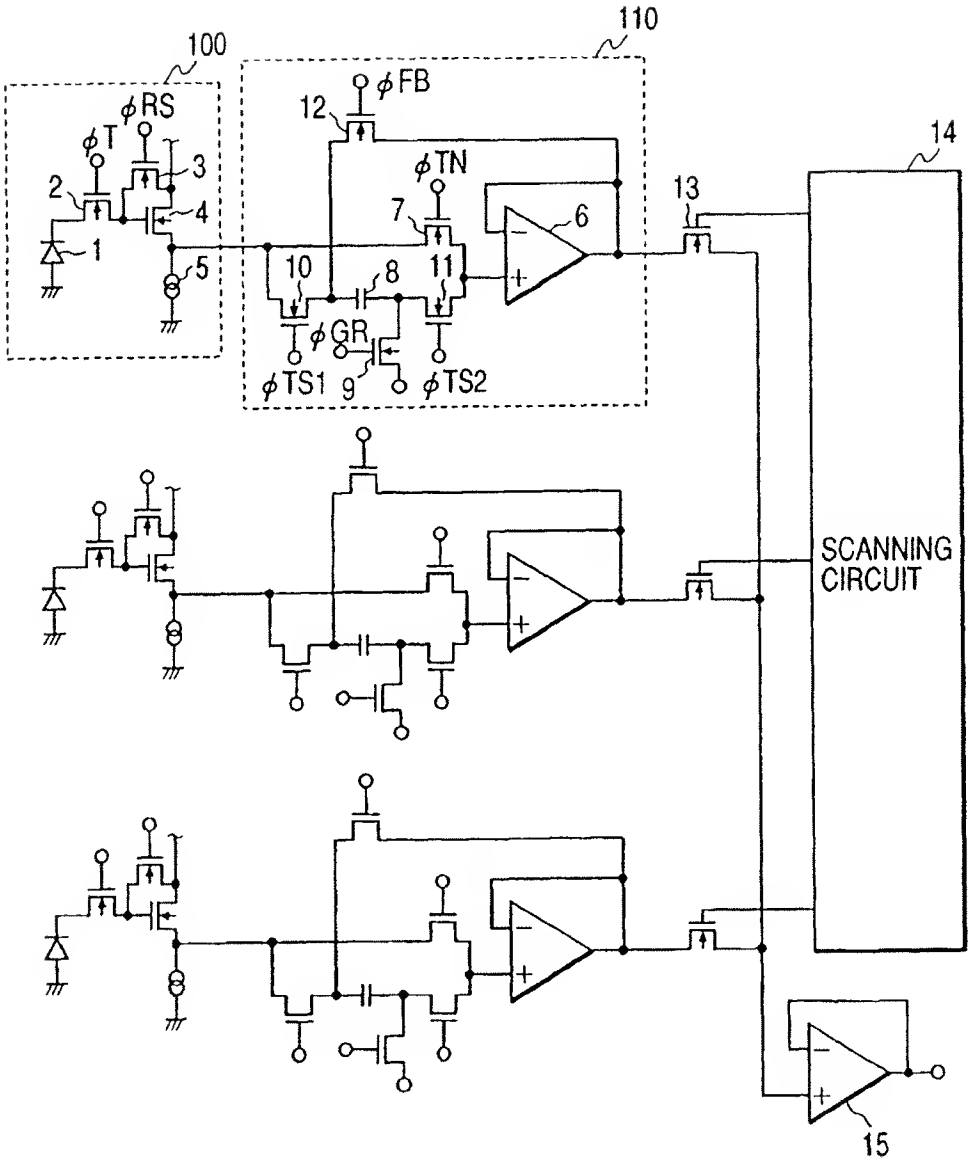

100
110
φRS
φT
φFB
φTN
φGR
φTS1
φTS2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
SCANNING CIRCUIT

FIG. 4

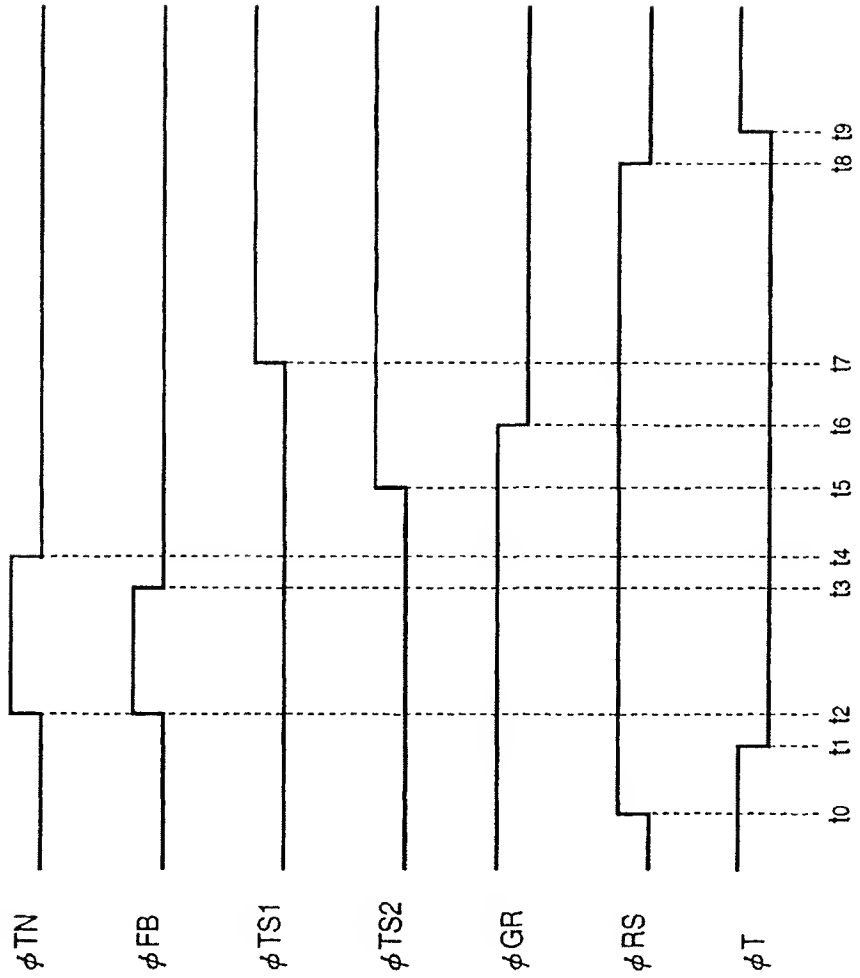


FIG. 5

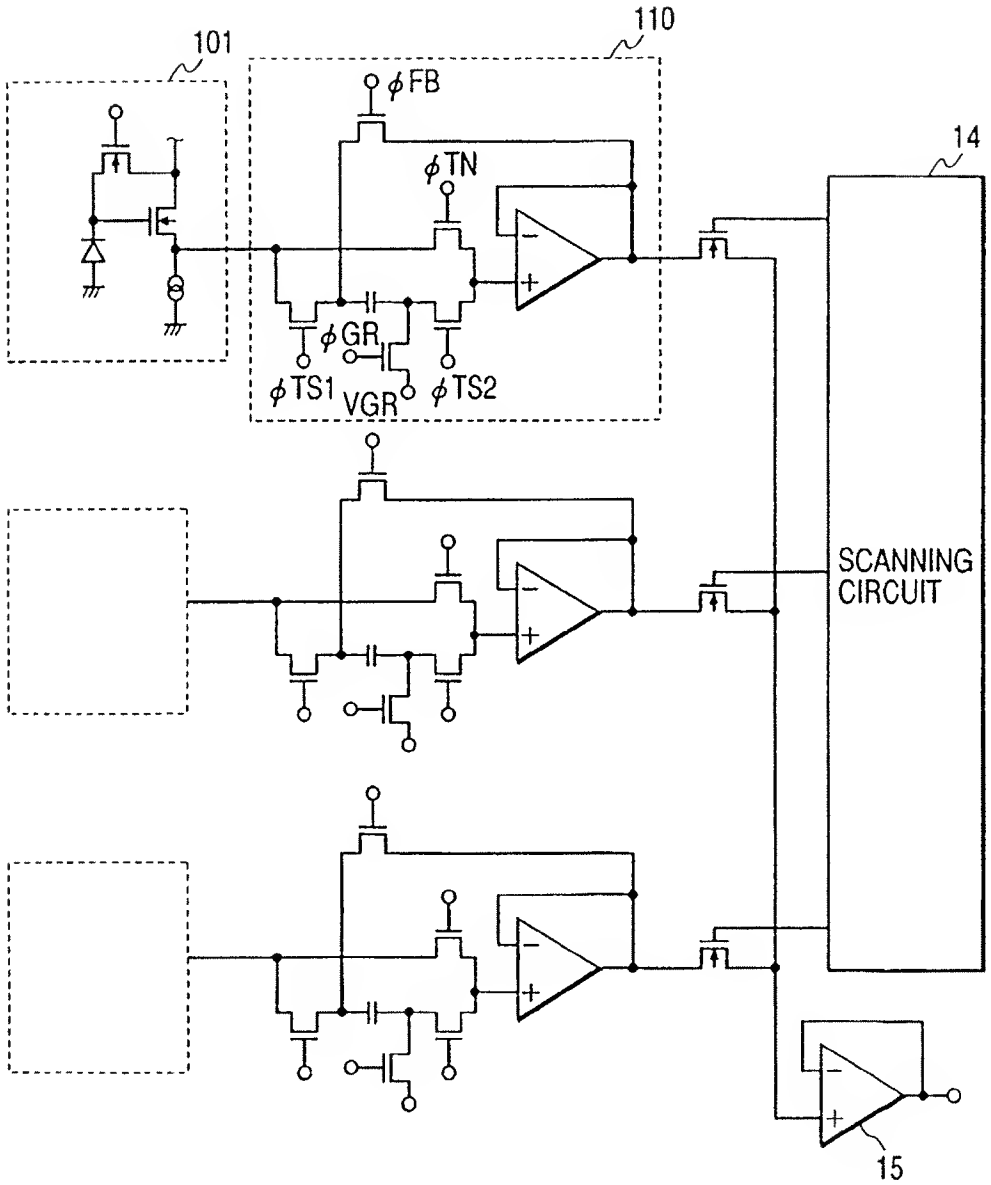


FIG. 6

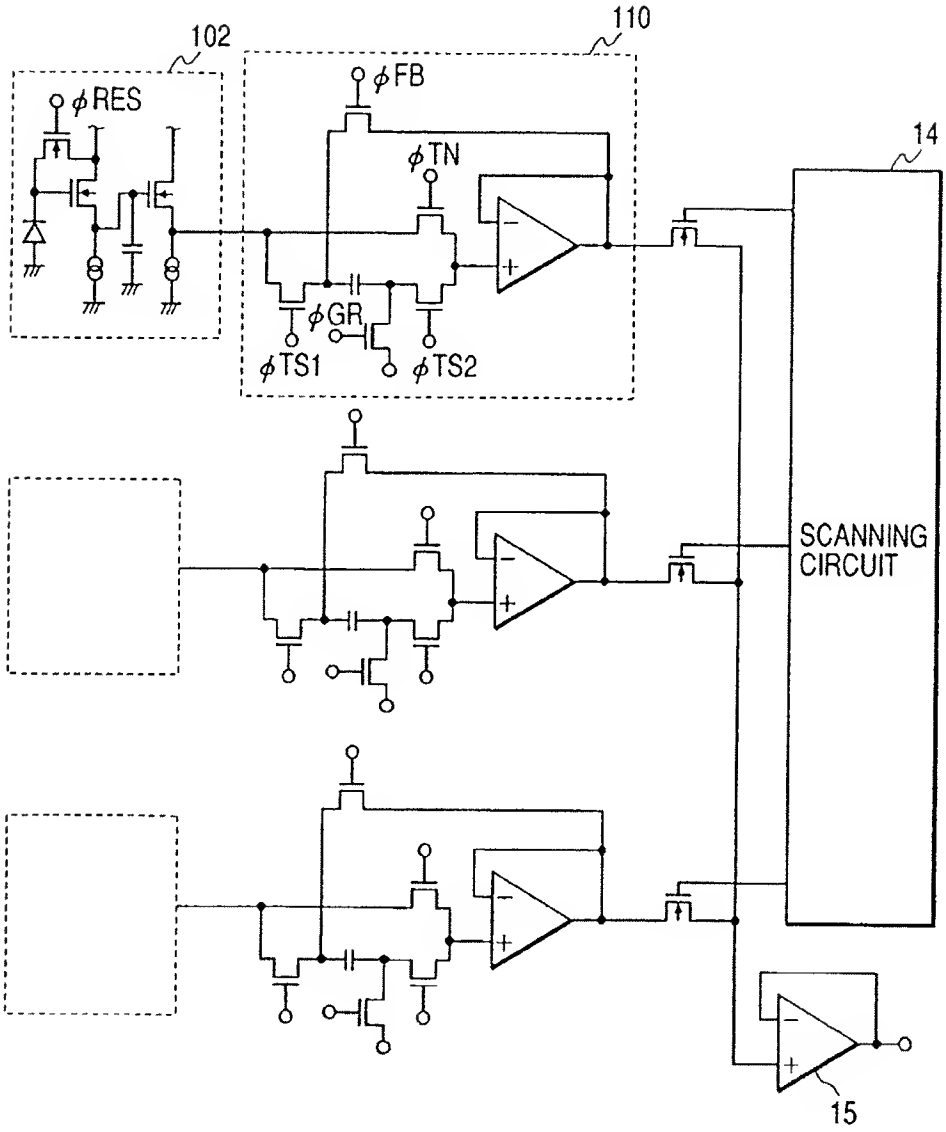


FIG. 7

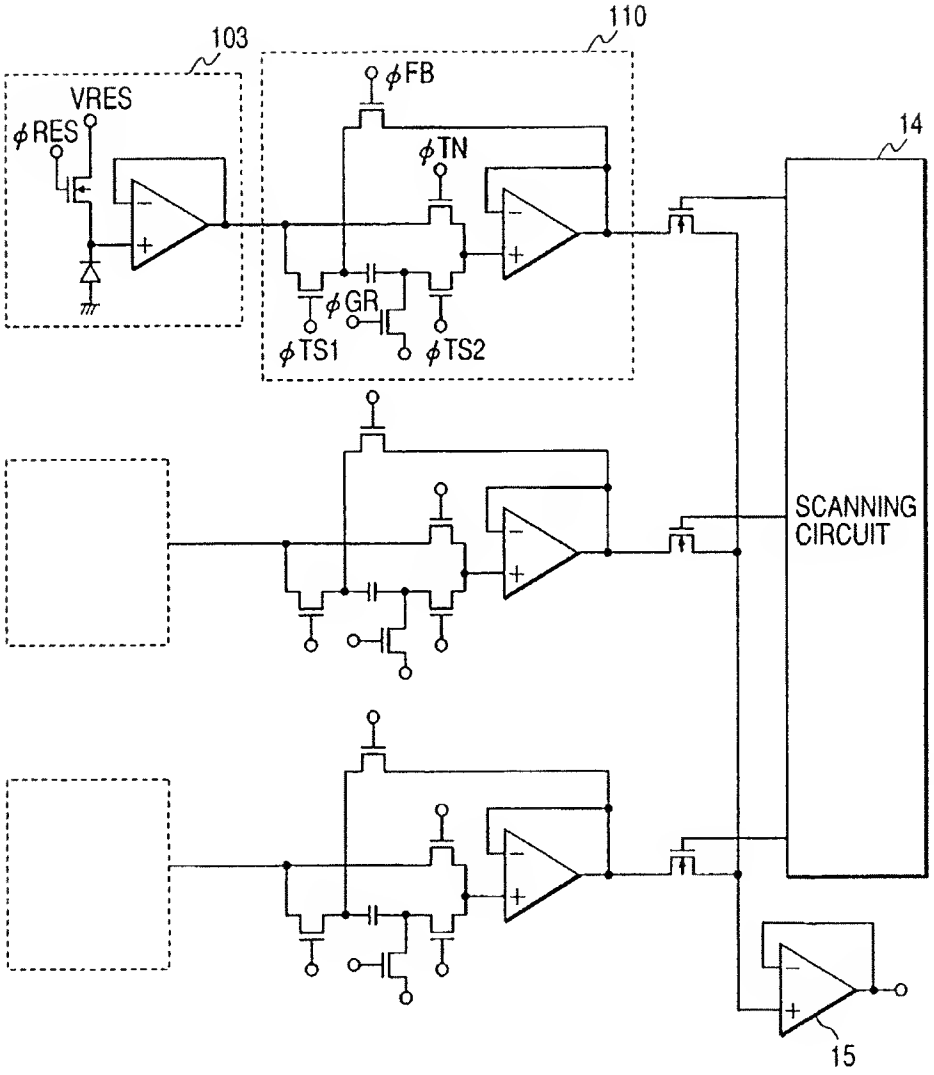

103
110
VRES
φRES
φFB
φTN
φGR
φTS1
φTS2
14
SCANNING CIRCUIT
15

FIG. 8

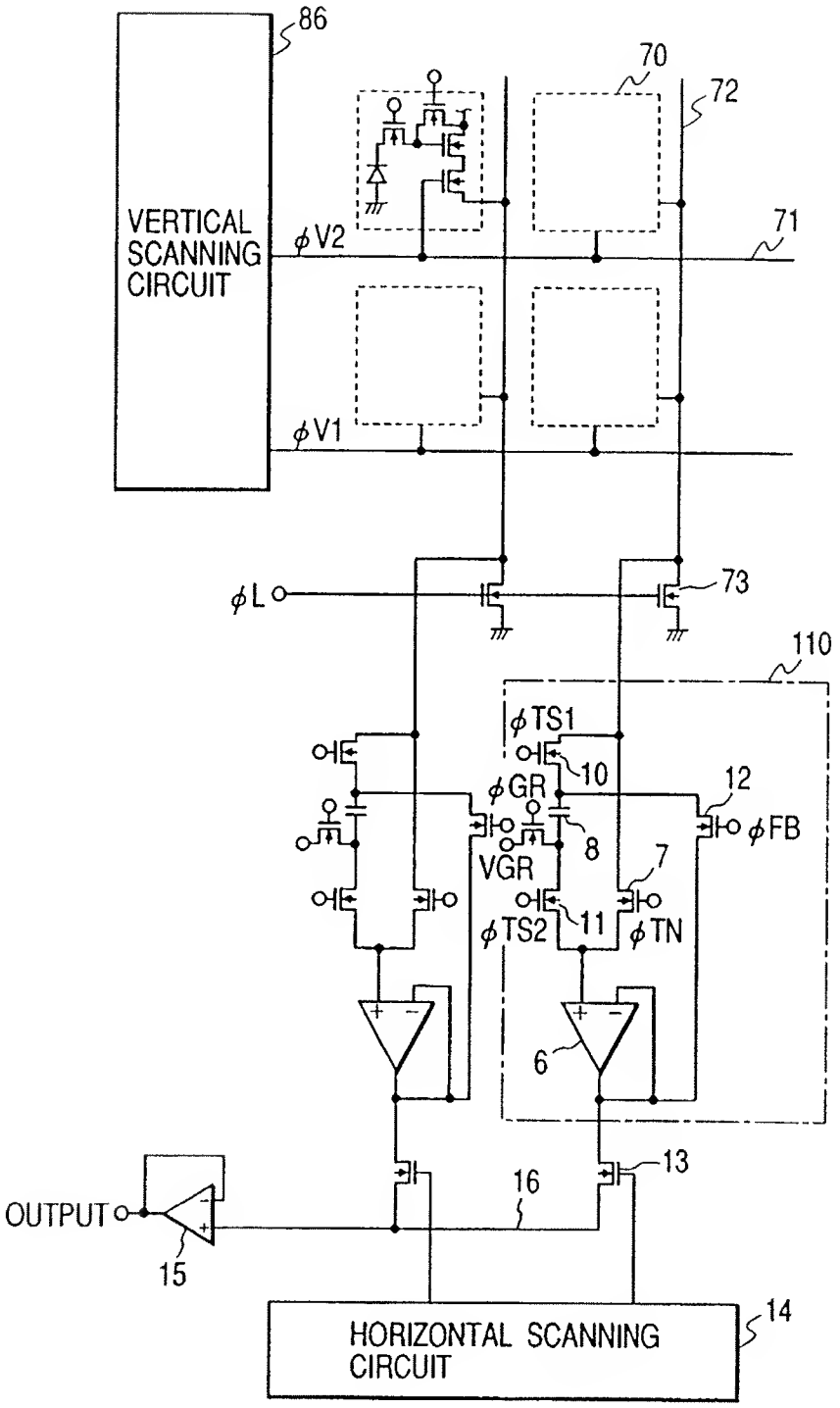

86
70
72
VERTICAL SCANNING CIRCUIT
φV2
71
φV1
φL
73
110
φTS1
10
φGR
12
φFB
8
VGR
7
φTS2
11
φTN
6
OUTPUT
15
16
13
HORIZONTAL SCANNING CIRCUIT
14

FIG. 9A

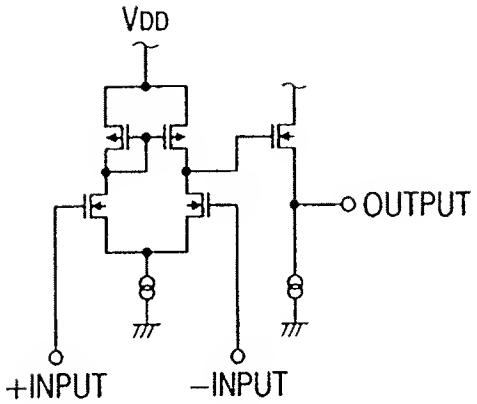


FIG. 9B

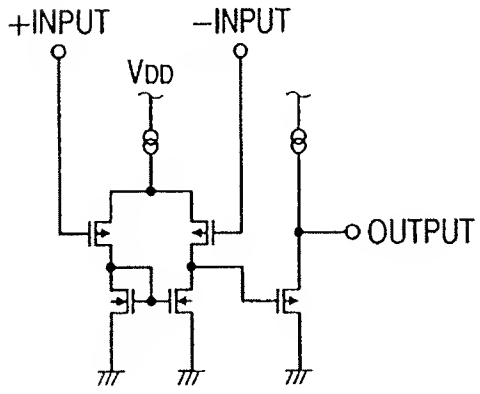


FIG. 10

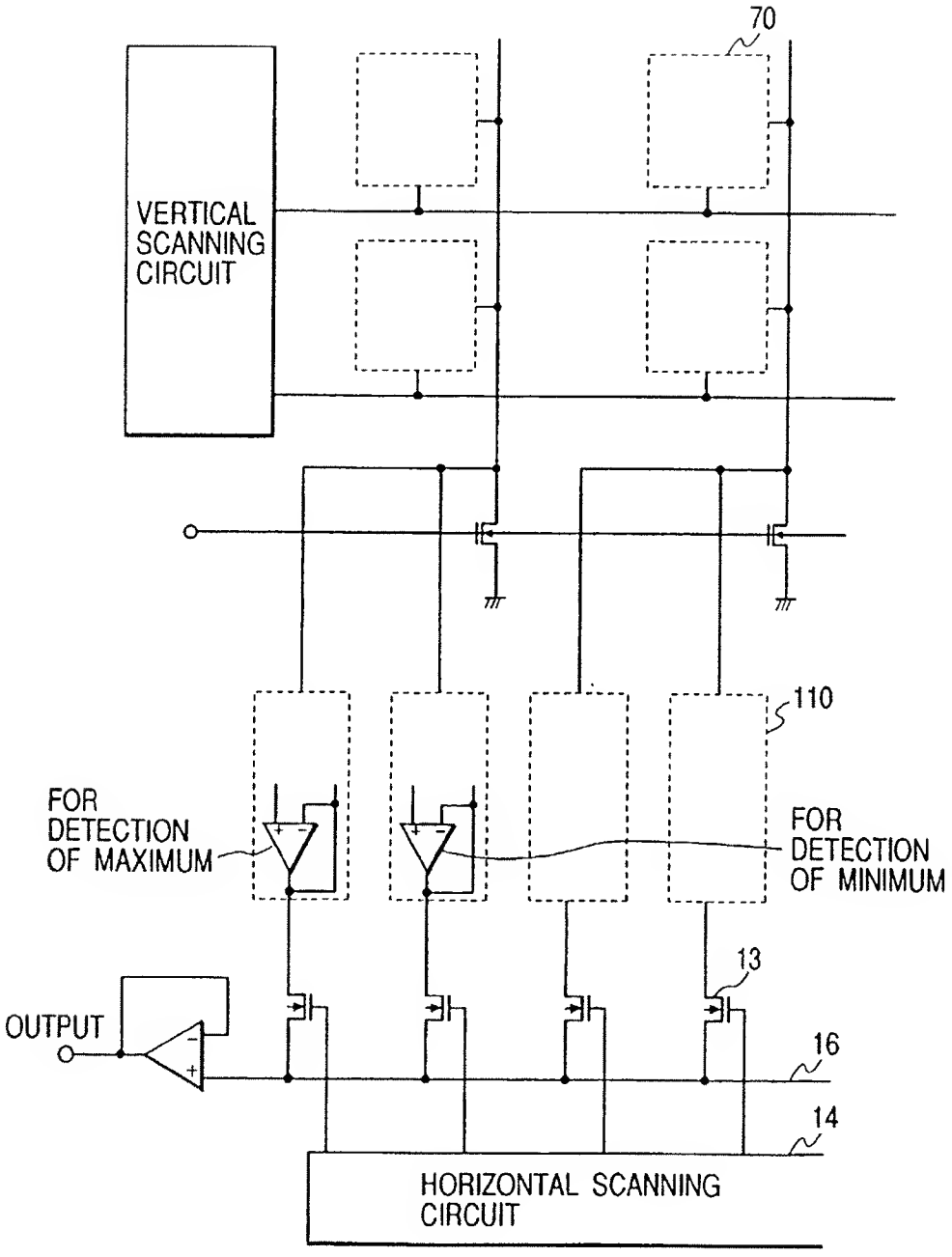

70
VERTICAL SCANNING CIRCUIT
110
FOR DETECTION OF MAXIMUM
FOR DETECTION OF MINIMUM
13
OUTPUT
16
14
HORIZONTAL SCANNING CIRCUIT

FIG. 11

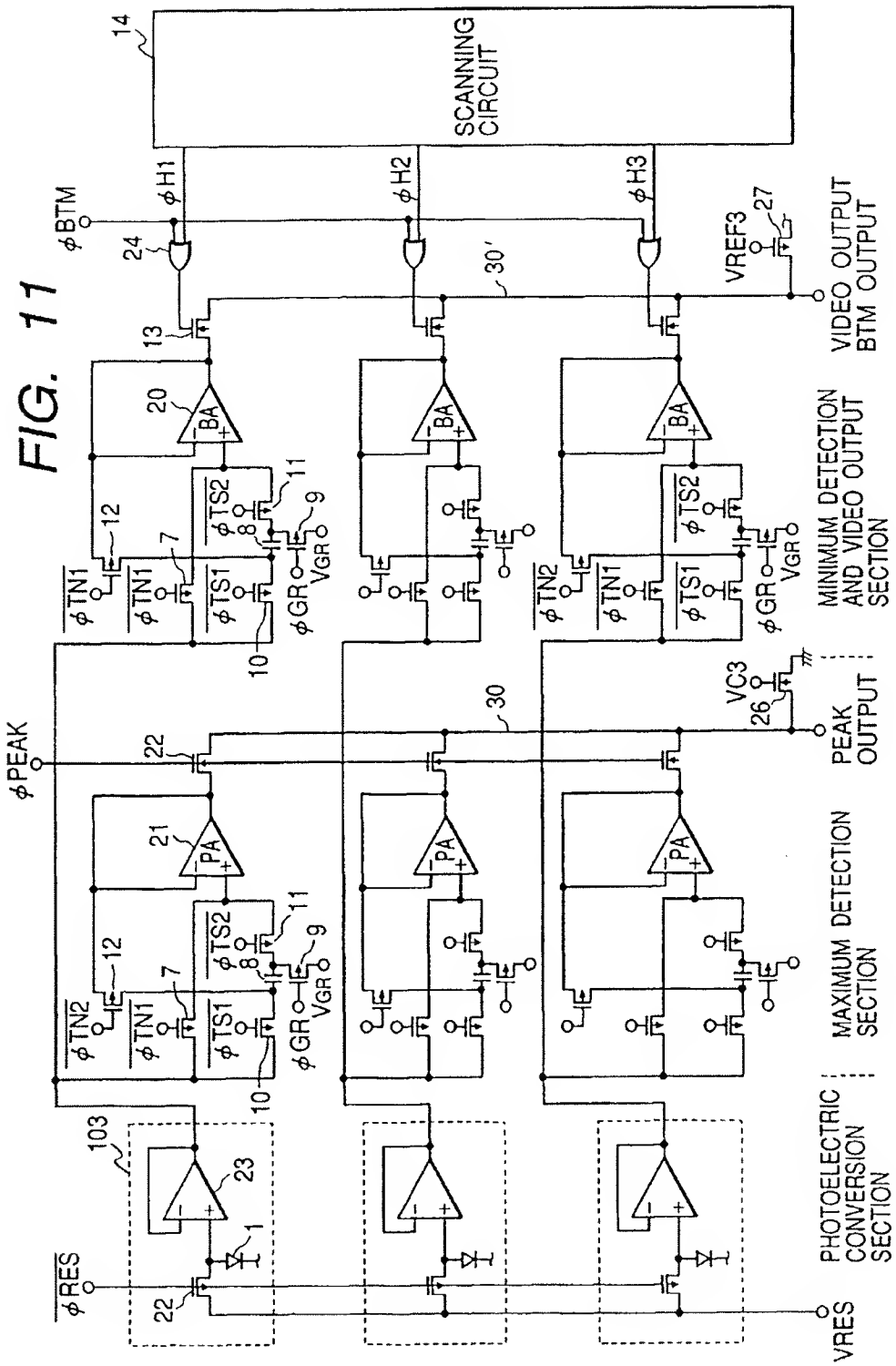

SCANNING CIRCUIT
14
φH1
φH2
φH3
φBTM
24
30'
VREF3
27
VIDEO OUTPUT
BTM OUTPUT
13
20
BA
12
7
8
11
9
10
φTN1
φTS1
φTS2
φGR
VGR
MINIMUM DETECTION AND VIDEO OUTPUT SECTION
φPEAK
22
30
VC3
26
PEAK OUTPUT
21
PA
φTN2
MAXIMUM DETECTION SECTION
103
23
1
φRES
VRES
PHOTOELECTRIC CONVERSION SECTION

FIG. 12

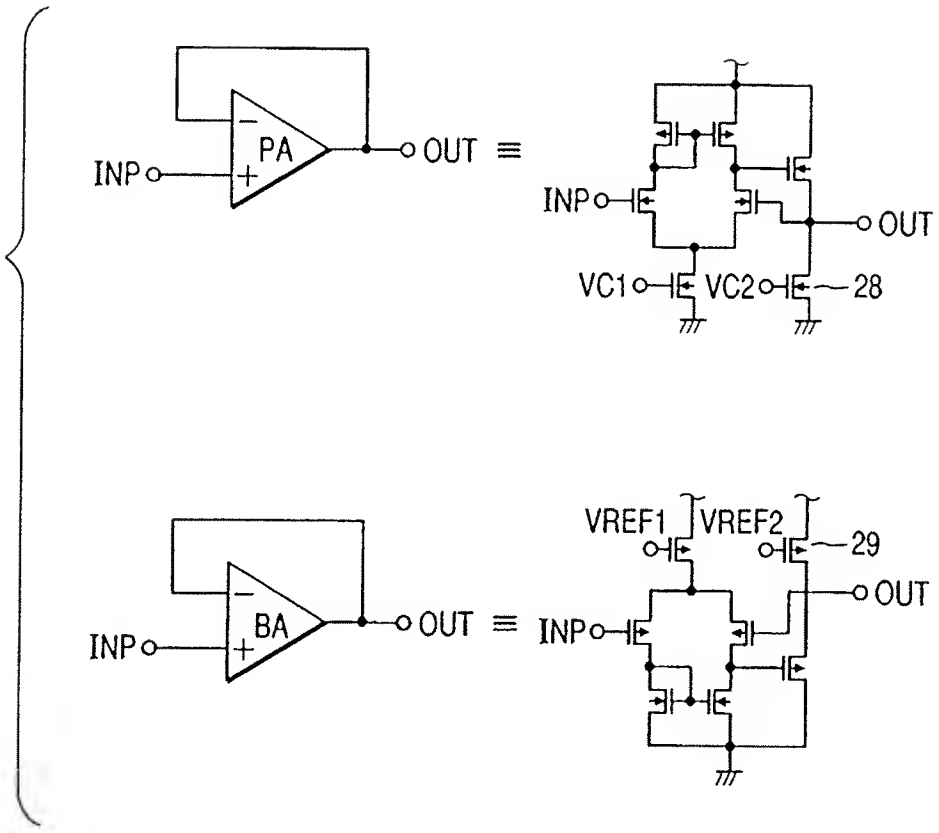


FIG. 13

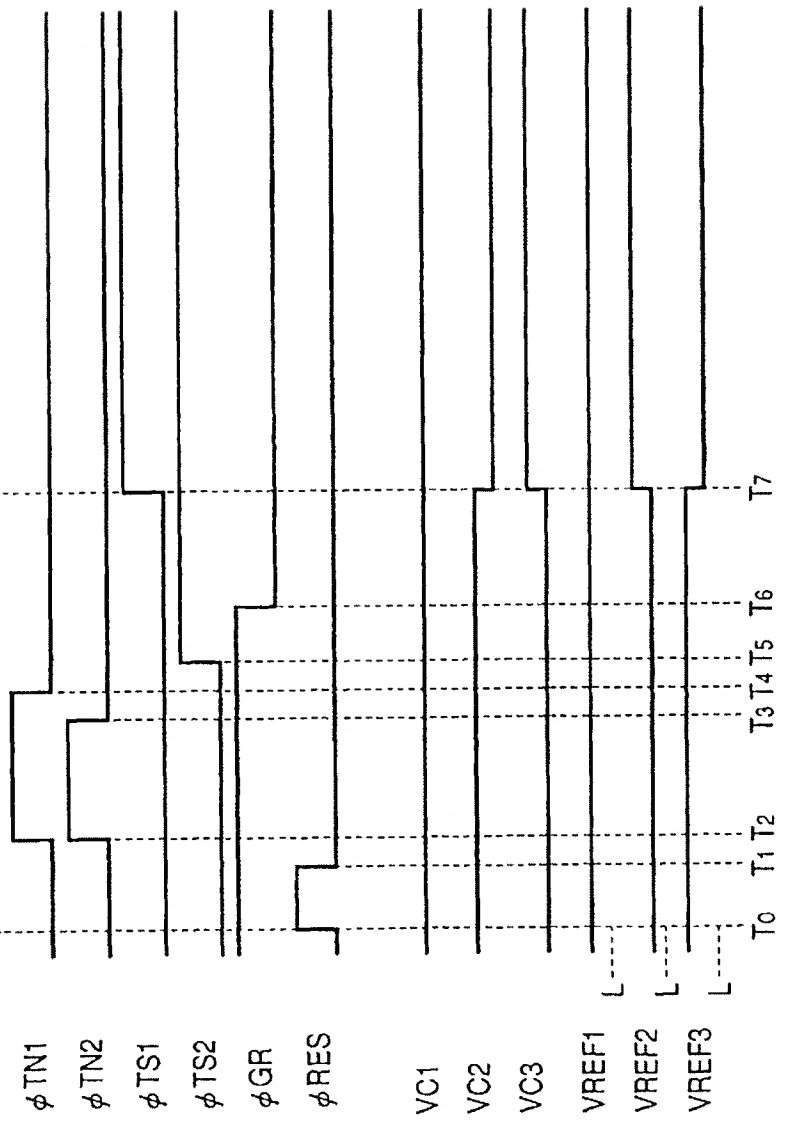

RESET PERIOD
AGC PERIOD
φTN1
φTN2
φTS1
φTS2
φGR
φRES
VC1
VC2
VC3
VREF1
VREF2
VREF3
T0
T1
T2
T3
T4
T5
T6
T7

FIG. 14

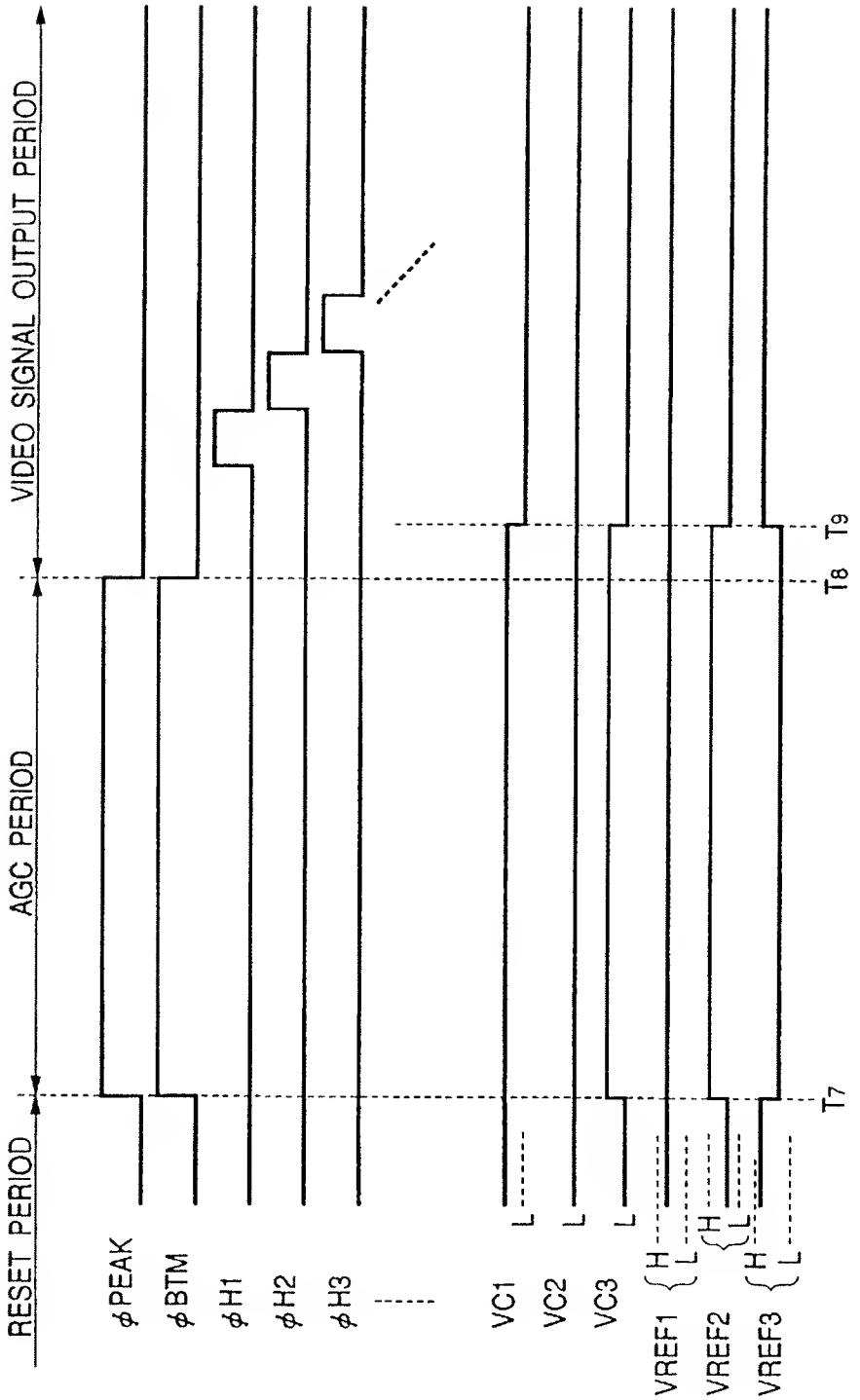

VIDEO SIGNAL OUTPUT PERIOD
AGC PERIOD
RESET PERIOD
φPEAK
φBTM
φH1
φH2
φH3
VC1
VC2
VC3
VREF1
VREF2
VREF3
H
L
T7
T8
T9

FIG. 15

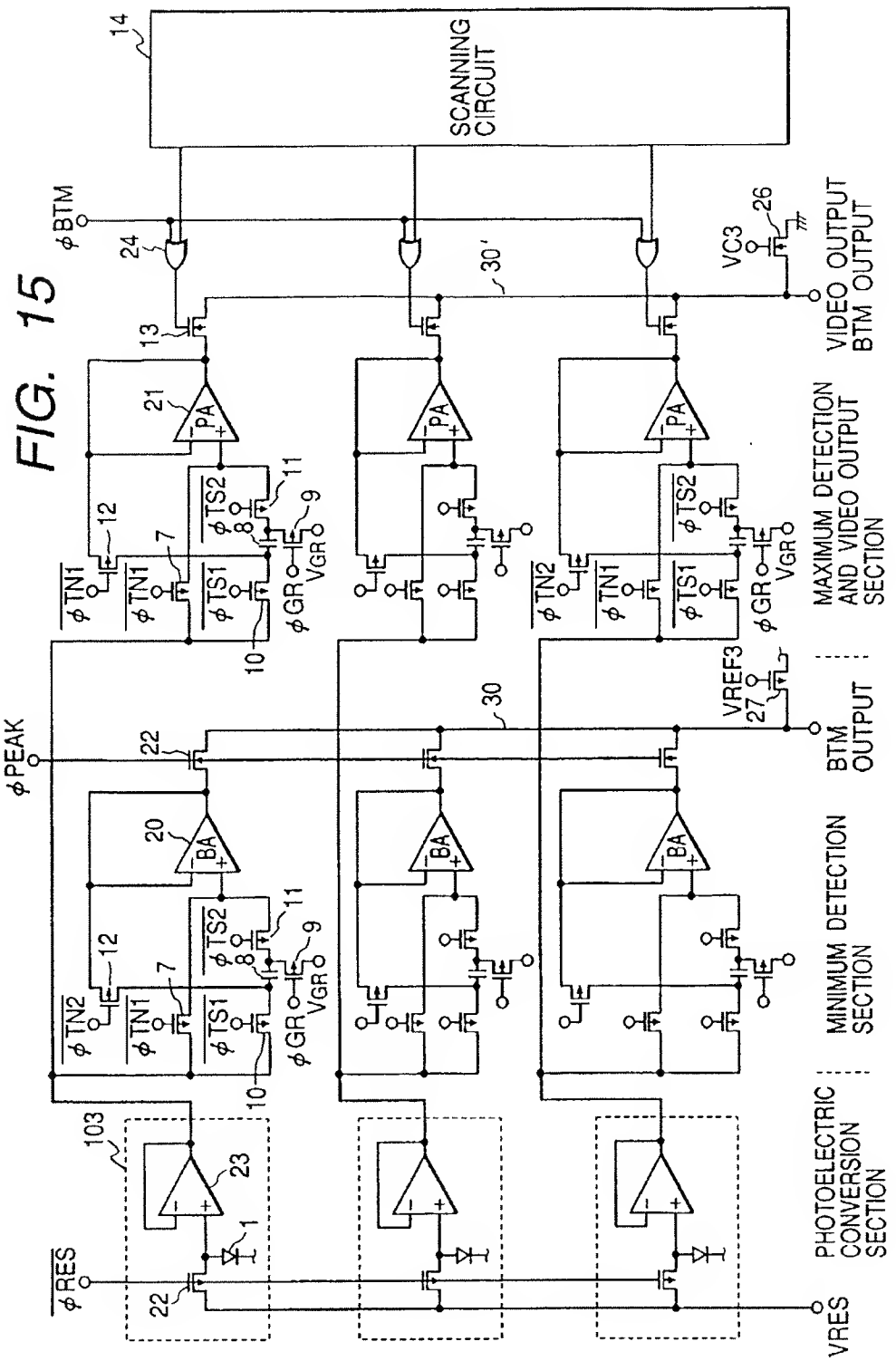

SCANNING CIRCUIT
14
φBTM
24
30'
VC3
26
VIDEO OUTPUT
BTM OUTPUT
13
21
PA
12
7
11
9
10
φTN1
φTS1
φTS2
φGR
VGR
MAXIMUM DETECTION AND VIDEO OUTPUT SECTION
VREF3
27
φPEAK
22
30
BTM OUTPUT
20
BA
φTN2
MINIMUM DETECTION SECTION
103
23
1
φRES
VRES
PHOTOELECTRIC CONVERSION SECTION

FIG. 16

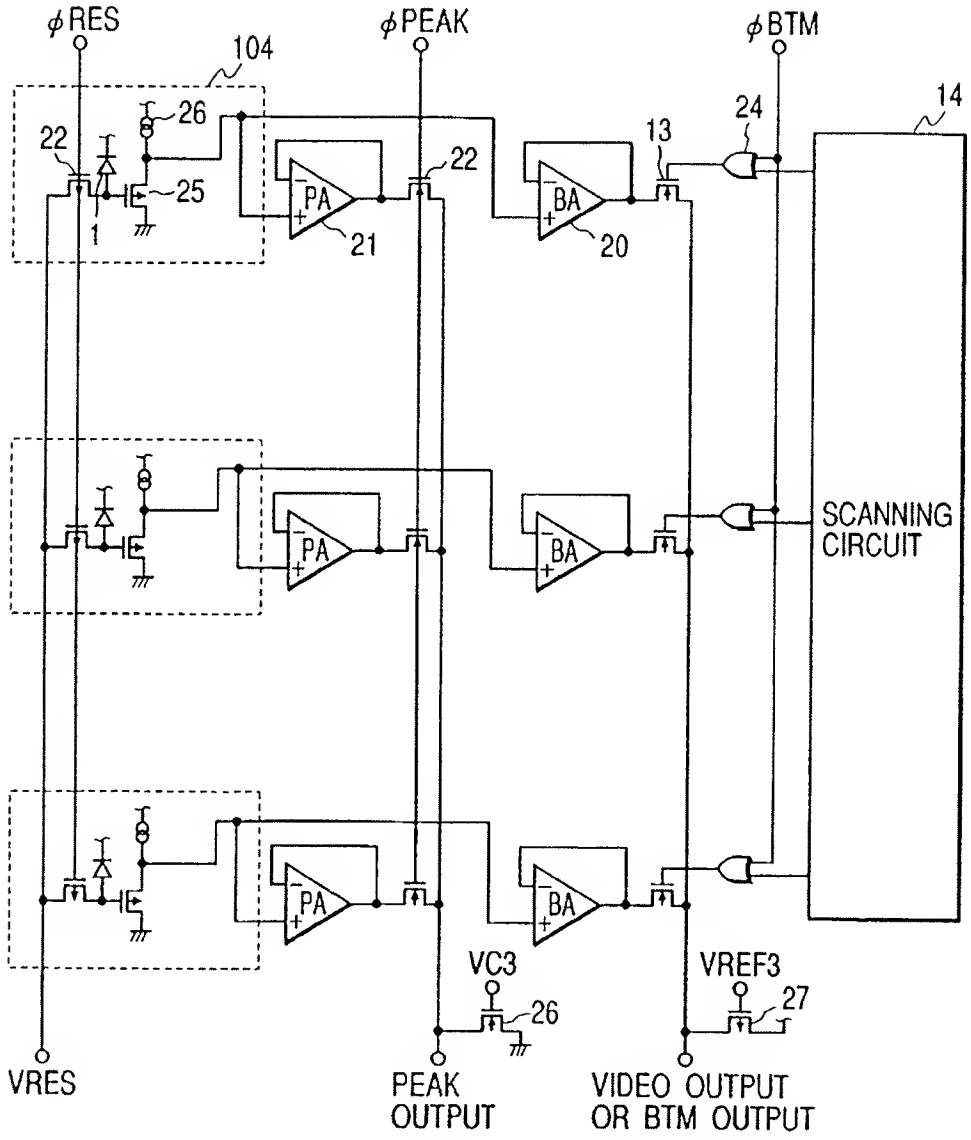

φRES
φPEAK
φBTM
104
26
22
25
1
PA
21
22
BA
20
13
24
14
SCANNING CIRCUIT
VC3
26
VREF3
27
VRES
PEAK OUTPUT
VIDEO OUTPUT OR BTM OUTPUT

FIG. 17

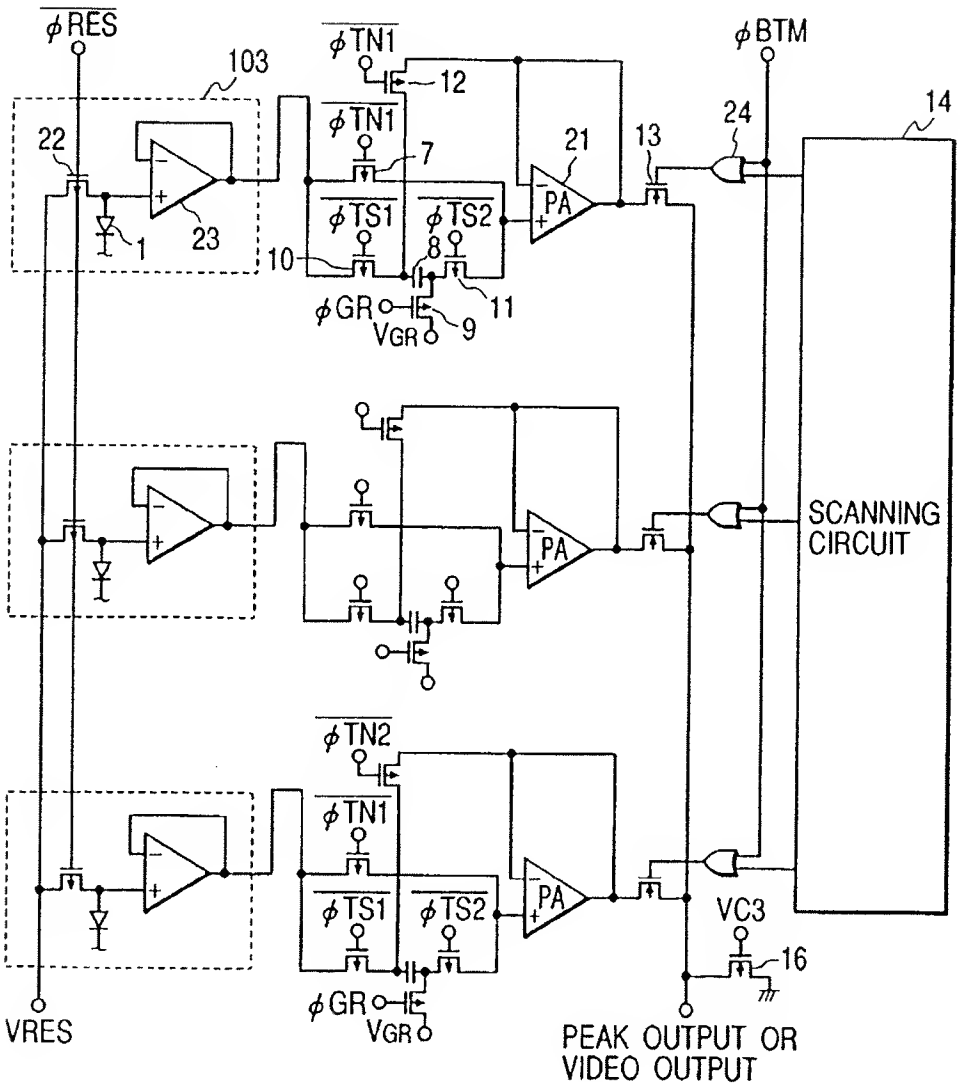

φRES
103
φTN1
12
φBTM
14
22
φTN1
7
21
13
24
φTS1
φTS2
PA
1
23
10
8
11
φGR
VGR
9
SCANNING CIRCUIT
φTN2
φTN1
φTS1
φTS2
VC3
16
VRES
φGR
VGR
PEAK OUTPUT OR VIDEO OUTPUT

FIG. 18

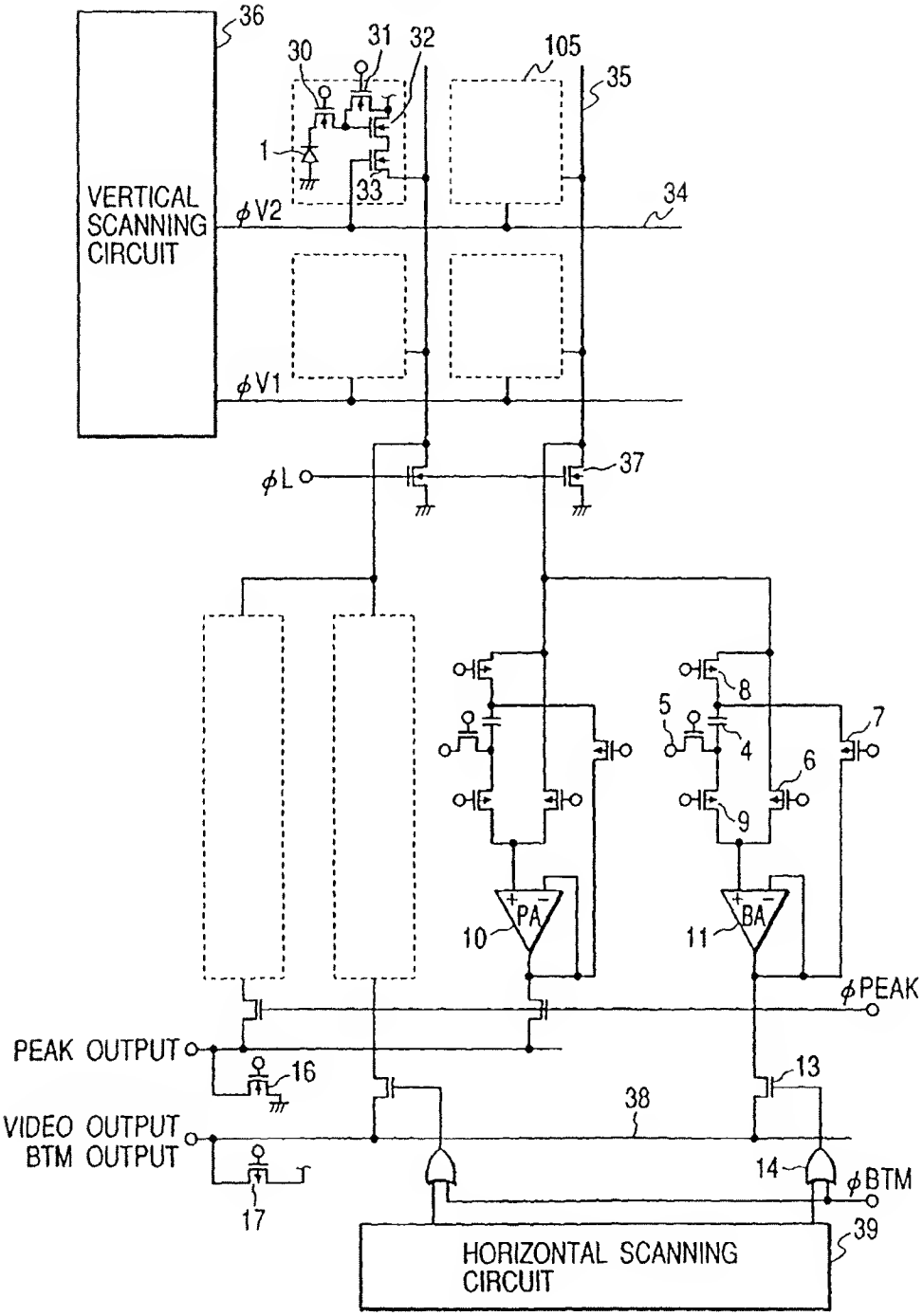

36
VERTICAL SCANNING CIRCUIT
30
31
32
105
35
1
33
34
φV2
φV1
φL
37
8
5
4
7
6
9
10
PA
11
BA
φPEAK
PEAK OUTPUT
16
13
38
VIDEO OUTPUT
BTM OUTPUT
17
14
φBTM
39
HORIZONTAL SCANNING CIRCUIT

FIG. 19

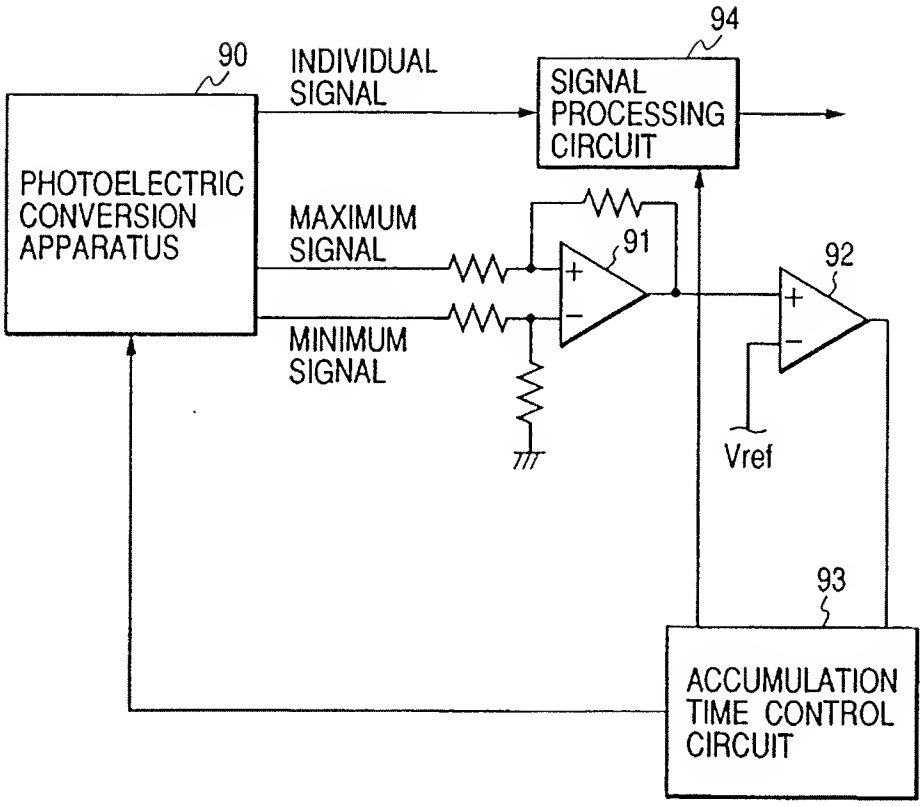
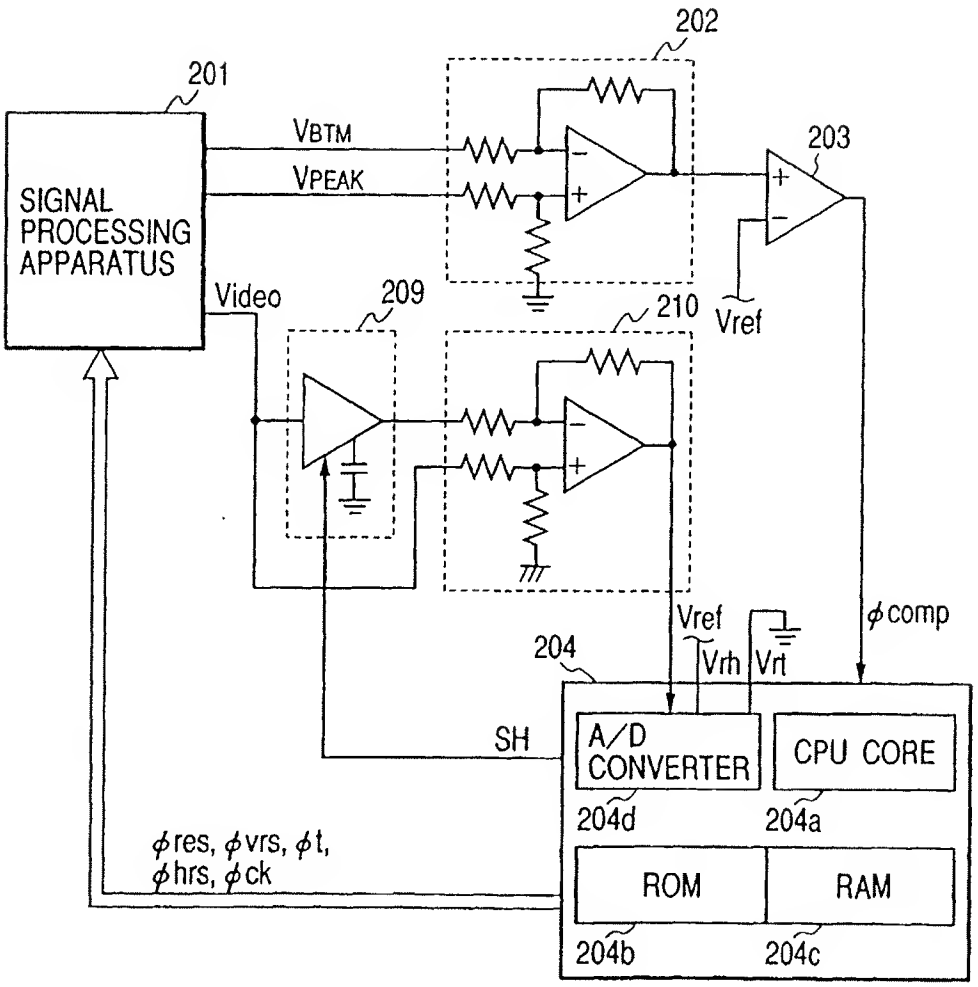

90
INDIVIDUAL SIGNAL
94
SIGNAL PROCESSING CIRCUIT
PHOTOELECTRIC CONVERSION APPARATUS
MAXIMUM SIGNAL
MINIMUM SIGNAL
91
92
Vref
93
ACCUMULATION TIME CONTROL CIRCUIT

FIG. 20


202
201
VBTM
VPEAK
203
SIGNAL PROCESSING APPARATUS
Video
209
210
Vref
Vref
Vrh
Vrt
φcomp
204
SH
A/D CONVERTER
CPU CORE
204d
204a
φres, φvrs, φt,
φhrs, φck
ROM
RAM
204b
204c